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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/688,803	10/17/2000	Yoshiyuki Nakamura	088941/0173	2065

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EXAMINER
WHITTINGTON, ANTHONY T

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 04/22/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/688,803	NAKAMURA, YOSHIYUKI	
	Examiner	Art Unit	
	Anthony T Whittington	2133	

-- Th MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Peri d for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 February 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *3* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Rejection under 35 U.S.C. 102(e), Patent to Another with Earlier Filing Date, Reference is a U.S. Patent Issued Directly or Indirectly From a National Stage of, or a Continuing Application Claiming benefit under 35 U.S.C. 365(c) to, an International Application Having an International Filing Date Prior to November 29, 2000

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

Claims 1, 2, 3,6,7,8,9,12 and 13 are rejected under 35 U.S.C. 102(b) as being anticipated by James (U.S. 5,678,289).

As per claims 1 and 9, James teaches a test circuit and a method that is provided between a first and second target circuits for testing the target circuits comprising all the elements of the instant application. James teaches a first selecting section (MUX, 41) for selecting and outputting

one of a first output signal (Serial Data In) and a second output signal (Normal Data In) in Figure 8. In Figure 8, James also teaches a test signal (SHIFTDR) indicating a test pattern input that is according to first and second test mode signals (MODE TEST/NORMAL, Figure 6). James teaches a temporary data storage section (43) for temporarily storing the signal selected by the first section as a data signal in Figure 6. James teaches a second selecting circuit (MUX, 47) for selecting one of the temporarily stored data signal or the second output signal (SERIAL DATA IN) according to the second test mode signal (MODE TEST/NORMAL) that provides the selected signal to the first target circuit in Figure 6. James teaches a third selecting section (MUX, 66) for selecting one of the temporarily stored data signal or the first output signal from the first target circuit according to a third test mode signal (CELL BYPASS) in Figure 6. James teaches a temporarily stored data signal (signal stored in latch 43) that is also output as a test result via a test pattern output terminal.

As per claim 2, James teaches a test circuit (Boundary-SCAN CELL, Figure 3) in Figure 1. Figure 3 shows the typical IC device for testing as stated in column 24, lines 21-67.

As per claim 3, James teaches the first (41), second (47) and third (66) selecting sections are multiplexers in Figure 6.

As per claims 6 and 8, James teaches a system for forming test circuits for testing an integrated circuit device comprising all the elements of the instant application. James teaches a test circuit forming section (Boundary-SCAN CELL) for forming test circuits in Figure 3. James teaches a core connecting section (IC CORE LOGIC, 6) for connecting each test circuit in Figure 1. James teaches a serial connecting section (51) for connecting an external terminal of the

integrated circuit device so as to form a serial chain of a predetermined number of test circuits wherein a test result is output from the test pattern output terminal (output stage, 24) in Figure 5.

As per claim 7, James teaches a system of forming test circuits comprising all the elements of the instant application. James teaches a parallel-connecting section (51 and 53) for providing separated serial chains in Figure 5. James teaches also in Figure 5 a test signal (TDI) is supplied to each serial chain provided by the parallel-connecting section.

As per claim 12, James teaches a computer readable storage medium storing a program for making a computer execute an operation of forming test circuits for testing an integrated circuit device, the operation comprising all the elements of the instant application.
James teaches test circuit (Boundary-SCAN CELL) forming step of forming test circuits in Figure 3. James teaches a core connecting step (IC CORE LOGIC, 6) for connecting each test circuit in Figure 1. James teaches a serial connecting step (51) for connecting an external terminal of the integrated circuit device so as to form a serial chain of a predetermined number of test circuits wherein a test result outputting step of outputting a test result from the test pattern output terminal (output stage, 24) in Figure 5.

As per claim 13, James teaches a computer readable storage medium comprising all the elements of the instant application. . James teaches a parallel-connecting step (51 and 53) of providing separated serial chains in Figure 5. James teaches also in Figure 5 a test signal (TDI) supplying step that is supplied to each serial chain provided in the parallel-connecting step. James teaches a test result outputting step of outputting a test result from the test pattern output terminal (output stage, 24) in Figure 5.

Claims 4,5, 10, 11,14 and 15 are rejected under 35 U.S.C. 102(e) as being anticipated by Asaka (U.S. 6,189,128).

As per claim 4, Asaka teaches a system of forming test circuits for testing target circuits in an integrated circuit device comprising all the elements of the instant application. Asaka teaches a parallel number calculating section (first calculator, 651), a serial length calculating section (second calculator, 652) and a detecting section (selection processor, 65) that are equivalent to the instant application in Figure 10. In column 10, lines 8-34, Asaka teaches that each calculator calculates a candidate of scan paths (number of input-output chains) for cases of forming candidate scan paths by replacing each register of a plurality of appropriated paths by a scan element. As seen from Figure 3, a candidate of scan paths (number of input-output chains) includes serial and parallel scan paths. Therefore, each calculator has the ability to calculate parallel number and serial length calculations. In Figure 14, Asaka shows the steps by the detecting section (selection processor, 65,Figure 10) to compare the number of input terminals and the number of output terminals of each target circuit.

As per claim 5, Asaka teaches a system of forming test circuits for testing target circuits in an integrated circuit device comprising all the elements of the instant application. Asaka teaches a parallel number calculating section (first calculator, 651), a common serial length calculating section (second calculator, 652) and a detecting section (selection processor, 65) that are equivalent to the instant application in Figure 10. In column 10, lines 8-34, Asaka teaches that each calculator calculates a candidate of scan paths (number of input-output chains) for cases of forming candidate scan paths by replacing each register of a plurality of appropriated paths by a scan element. As seen from Figure 3, a candidate of scan paths (number of input-

output chains) includes serial and parallel scan paths. Therefore, each calculator has the ability to calculate parallel number and common serial length calculations. In Figure 14, Asaka shows the steps by the detecting section (selection processor, 65,Figure 10) to compare the number of input terminals and the number of output terminals of each target circuit. Asaka also shows in Figure 14 detecting a maximum number (determining all appropriated paths been extracted, T4) as a compared result.

As per claim 10, Asaka teaches a method of forming test circuits for testing target circuits in an integrated circuit device comprising all the elements of the instant application. Asaka teaches a parallel number calculating step (first calculator, 651), a serial length calculating step (second calculator, 652) and a detecting step (selection processor, 65) that are equivalent to the instant application in Figure 10. In column 10, lines 8-34, Asaka teaches that each calculating step calculates a candidate of scan paths (number of input-output chains) for cases of forming candidate scan paths by replacing each register of a plurality of appropriated paths by a scan element. As seen from Figure 3, a candidate of scan paths (number of input-output chains) includes serial and parallel scan paths. Therefore, each calculating step calculates the parallel number and serial length calculations. In Figure 14, Asaka shows the test chain determination steps by the detecting section (selection processor, 65,Figure 10) to compare the number of input terminals and the number of output terminals of each target circuit.

As per claim 11, Asaka teaches a method of forming test circuits for testing target circuits in an integrated circuit device comprising all the elements of the instant application. Asaka teaches a parallel number calculating step (first calculator, 651), a common serial length calculating step (second calculator, 652) and a detecting step (selection processor, 65) that are

equivalent to the instant application in Figure 10. In column 10, lines 8-34, Asaka teaches that each calculating step calculates a candidate of scan paths (number of input-output chains) for cases of forming candidate scan paths by replacing each register of a plurality of appropriated paths by a scan element. As seen from Figure 3, a candidate of scan paths (number of input-output chains) includes serial and parallel scan paths. Therefore, each calculating step calculates the parallel number and common serial length calculations. In Figure 14, Asaka shows the test chain determination steps by the detecting section (selection processor, 65, Figure 10) to compare the number of input terminals and the number of output terminals of each target circuit.

As per claim 14, Asaka teaches a computer readable storage medium storing a program for making a computer execute an operation of forming test circuits for testing an integrated circuit device, the operation comprising all the elements of the instant application. Asaka teaches a parallel number calculating step (first calculator, 651), a serial length calculating step (second calculator, 652) and a detecting step (selection processor, 65) that are equivalent to the instant application in Figure 10. In column 10, lines 8-34, Asaka teaches that each calculating step calculates a candidate of scan paths (number of input-output chains) for cases of forming candidate scan paths by replacing each register of a plurality of appropriated paths by a scan element. As seen from Figure 3, a candidate of scan paths (number of input-output chains) includes serial and parallel scan paths. Therefore, each calculating step calculates the parallel number and serial length calculations. In Figure 14, Asaka shows the test chain determination steps by the detecting section (selection processor, 65,Figure 10) to compare the number of input terminals and the number of output terminals of each target circuit.

As per claim 15, Asaka teaches a computer readable storage medium storing a program for making a computer execute an operation of forming test circuits for testing an integrated circuit device, the operation comprising all the elements of the instant application. Asaka teaches a parallel number calculating step (first calculator, 651), a common serial length calculating step (second calculator, 652) and a detecting step (selection processor, 65) that are equivalent to the instant application in Figure 10. In column 10, lines 8-34, Asaka teaches that each calculating step calculates a candidate of scan paths (number of input-output chains) for cases of forming candidate scan paths by replacing each register of a plurality of appropriated paths by a scan element. As seen from Figure 3, a candidate of scan paths (number of input-output chains) includes serial and parallel scan paths. Therefore, each calculating step calculates the parallel number and common serial length calculations. In Figure 14, Asaka shows the test chain determination steps by the detecting section (selection processor, 65,Figure 10) to compare the number of input terminals and the number of output terminals of each target circuit.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The following patents are cited to further show the state of art with respect to parallel scan chain testing in general:

U.S. Pat No. 6,079,039 to Nakamura

U.S. Pat No. 5,627,841 to Nakamura

U.S. Pat No. 5,680,406 to Nakamura

U.S. Pat No. 6,000,051 to Nadeau-Dostie et al.

U.S. Pat No. 6,223,315 to Whetsel

U.S. Pat No. 6,122,762 to Kim

U.S. Pat No. 5,960,008 to Osawa et al.

U.S. Pat No. 6,324,662 to Haroun et al.

U.S. Pat No. 5,710,867 to Giacalone et al.

U.S. Pat No. 6,134,675 to Raina

U.S. Pat No. 5,847,561 to Whetsel

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anthony T Whittington whose telephone number is 703-306-5617. The examiner can normally be reached on Monday-Friday 7:30a.m.-4:00p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on 703-305-9595. The fax phone numbers for the organization where this application or proceeding is assigned are 703-746-7239 for regular communications and 703-746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

A.W.
April 18, 2003

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